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Ambipolar Molybdenum Diselenide Field-Effect Transistors: Field-Effect and Hall Mobilities

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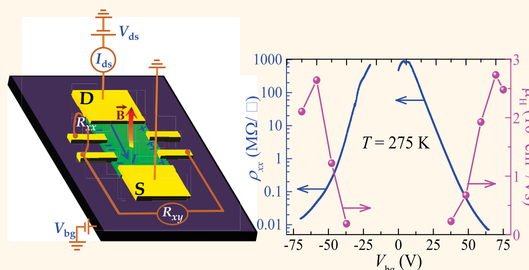
ABSTRACT We report a room temperature study on the electrical response of field-effect transistors (FETs) based on few-layered $MoSe_2$, grown by a chemical vapor transport technique, mechanically exfoliated onto SiO_2. In contrast to previous reports on $MoSe_2$ FETs electrically contacted with Ni, $MoSe_2$ FETs electrically contacted with Ti display ambipolar behavior with current on to off ratios up to 10^6 for both hole and electron channels when applying a small excitation voltage. A rather small hysteresis is observed when sweeping the back-gate voltage between positive and negative values, indicating the near absence of charge "puddles". For both channels the Hall effect indicates Hall mobilities $\mu_H \simeq 250$ cm^2/(V s), which are comparable to the corresponding field-effect mobilities, *i.e.*, $\mu_{FE} \sim 150$ to 200 cm^2/(V s) evaluated through the conventional two-terminal field-effect configuration. Therefore, our results suggest that $MoSe_2$ could be a good candidate for *p*—*n* junctions composed of a single atomic layer and for low-power, complementary logic applications.



KEYWORDS: $MoSe_2$ · two-dimensional atomic layers · transition metal dichalcogenides · field-effect transistors · Hall effect · Hall mobility

Transition metal dichalcogenides of the form TMX_2 (where TM refers to a transition metal such as Mo, W, Nb, Hf, *etc*., and X is a chalcogen element, *i.e*., S, Se or Te) are layered materials characterized by strong in-plane covalent bonding and weak interplanar van der Waals coupling, which are exfoliable into two-dimensional layers composed of just a few or even a single atomic layer.[1,2] Field-effect transistors (FETs) based on transition metal dichalcogenides (TMDs), MoS_2 in particular, were shown to display large transconductance as a function of its gate voltage due to their low density of states at the Fermi level, significant ratios between the current "on" and "off" states (or $I_{ON}/I_{OFF} > 10^8$) owing to their large band gap (~1.2 to 1.8 eV), and sharp conductance thresholds, or "subthreshold swings" as sharp as ~60 mV/decade, indicating an enhanced gate control.[1]

Along with these electrical properties, the planarity of the layers based on TMDs makes their transistors viable candidates for low power applications.[3] High thermal stability, chemical inertness, transparency, flexibility, and relative inexpensiveness also make them ideal for low cost electronics. Besides the exploration of their remarkable optical properties,[4,5,6] much of the current effort in the field of TMDs is devoted to the understanding of their fundamental electronic properties when exfoliated in single- or few-layers. For example, when mechanically exfoliated onto SiO_2, MoS_2 and $MoSe_2$ were found to be electron-doped compounds[7,8] in contrast to WS_2 and WSe_2, which were found to display ambipolar behavior.[9−11] The metals used for the electrical contacts were claimed to play a major role in their response, presumably by defining the size of the Schottky barrier associated with their work function[12] and by pinning the chemical potential closer to either the conduction or the valence bands: in WSe_2, for example, Ni and Pd contacts were found to favor either electron or hole conduction respectively, while the deposition of Pd and Ni each at one of the current leads, produces an enhanced ambipolar response.[11]

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In addition, the combination of single-layer TMDs with dielectrics having a large dielectric constant such as HfO_2 or Al_2O_3, led to several reports[3,13−15] claiming a remarkable increase in carrier mobility, which would make this architecture potentially useful for liquid crystals and organic light emitting displays.[3] Notice that logical elements as well as integrated circuits based on MoS_2 have already been reported.[16,17]

The observed ambipolar response, or the capacity to dope the conducting channel with either electrons or holes through the field-effect, could make some of these TMDs ideal for complementary digital logic applications. In modern electronics complementary metal-oxide semiconductors (or CMOS) are widely used in microprocessors, microcontrollers, static RAM, and other digital logic circuits, as well as for several analog circuit applications such as image sensors, data converters, or highly integrated transceivers. In CMOS the "complementary-symmetry" term refers precisely to the fact that the typical digital design uses complementary and symmetrical pairs of *p*-type and *n*-type metal-oxide semiconductor field-effect transistors (MOSFETs) for the logic functions. CMOS based devices are known to display high noise immunity and are characterized by low power consumption, characteristics which have justified their incorporation into the vast majority of modern integrated circuits. Contrary to the current CMOS technology, TMDs open the possibility of fabricating complementary and symmetrical pairs of field-effect transistors on the same atomic layer(s) without the need of extra dopants in the material which compromises carrier mobility. Our results also indicate that one does not necessarily need distinct metals and concomitant work functions, to induce ambipolar behavior in transition metal dichalcogenides thus simplifying the fabrication process.

Here, and in contrast to ref 8, we show that field-effect transistors based multilayered (~10 atomic layers) $MoSe_2$ grown by a vapor transport technique and mechanically exfoliated onto SiO_2, can display ambipolar behavior at room temperature when using a standard combination of metals, *i.e.*, Au on Ti for *all* the electrical contacts. Notice that the 4.33 eV work-function of Ti is closely matched by the electron affinity of bulk $MoSe_2$, *i.e.*, (4.45 ± 0.11) eV.[18] This implies that the Fermi level of Ti is very close to the bottom of the conduction band of $MoSe_2$, and therefore that one should expect a rather small, if not negligible, Schottky barrier for electron conduction through the Ti:Au contacts. Remarkably, one extracts through Hall effect measurements, Hall mobilities in excess of 250 $cm^2/(V\ s)$ for both holes and electrons. These values are remarkable, since they are comparable or higher than most values reported so far for TMDs at room temperature[3,8,13−15,19] but are obtained without the use of high κ-dielectrics such as HfO_2, doping, or of a particular combination of metals for the electrical contacts. Although the room temperature mobilities previously reported to surpass 250 $cm^2/(V\ s)$ for other TMDs[12,14] have yet to be independently verified through Hall effect measurements, our results suggest that improvements in fabrication, *e.g.*, the choice of a more adequate substrate (*i.e.*, with low surface roughness, no dangling bonds, and with small amounts of spurious charges) and on the quality of the starting material (with a lower amount of defects) could make field-effect transistors based on few atomic layers of synthetic $MoSe_2$ excellent candidates for complementary logic electronics.

RESULTS AND DISCUSSION

Figure 1a shows an optical microscopy image of one of our devices based on multilayered $MoSe_2$ with a 7 contacts configuration, where 5 contacts can be used for 4 point resistivity as well as Hall resistance measurements and 2 contacts for current injection. For the four terminal measurements discussed here, the voltage was measured between voltage leads 1 and 2, and the Hall effect between voltage contacts 1 and 3. We checked that the results discussed below are consistent with results obtained in similar devices. Figure 1b displays a sketch of a typical $MoSe_2$ field-effect transistor depicting the configuration of measurements. Figure 1c shows an AFM image of the FET whose optical image is shown in Figure 1a. The thickness of the $MoSe_2$ crystal was measured by scanning the AFM tip along the blue line. Figure 1d shows the height profile from AFM measurements, indicating a thickness of ~7 nm or nearly 10 atomic layers.

Figure 2a shows the drain-source current I_{ds} normalized by the channel width w in a logarithmic scale and for several constant values of the excitation voltage V_{ds}, as a function of the back-gate voltage V_{bg}. In contrast to MoS_2 and to previous reports,[8] $MoSe_2$ shows ambipolar response, *i.e.*, a sizable electric-field-induced current for both positive (electrons accumulated at the interface) and negative (holes) gate voltages. Notice that for both positive and negative values of V_{bg}, I_{ds} approaches sizable currents of ~1 $\mu A/\mu m$ despite the relatively small maximum excitation voltage V_{ds} = 150 mV. Figure 2b shows I_{ds} as a function of V_{bg} for V_{ds} = 150 mV and for both increasing (blue line) and decreasing (magenta line) gate voltages. As seen, a small hysteresis is observed, which can be attributed to either a certain amount of Joule heating at the level of the contacts or to the pinning of either electrons or holes to spurious charges in the channel, leading to the formation of charge "puddles" with a gate-voltage dependent size. Here, the important observation is that this hysteresis is rather small indicating that the trapping or detrapping time is rather short.

Figure 3a displays drain-source current I_{ds} as a function of the excitation voltage V_{ds} for several values of the back-gate voltage V_{bg}. As seen, the response is approximately linear when V_{ds} < 200 mV, and for this

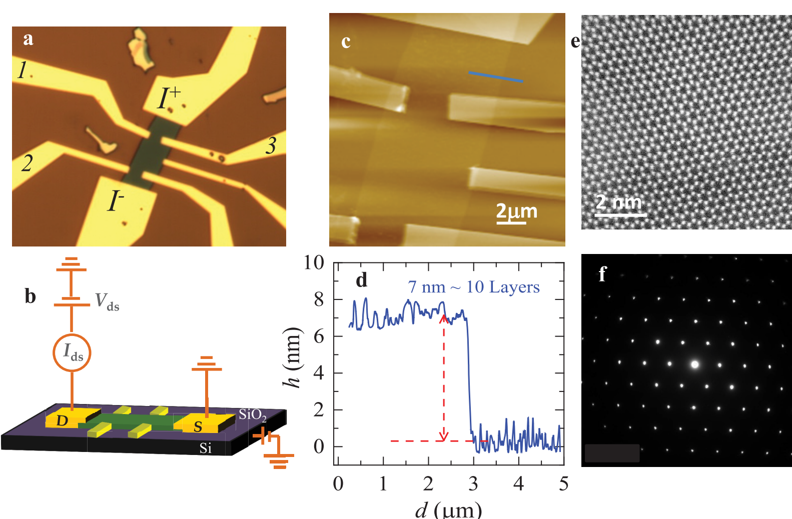

Figure 1. (a) Optical image of one of our multilayered $MoSe_2$ field-effect transistors. Gold pads correspond to voltage (pads labeled as 1, 2, 3, *etc.*) and current leads (pads labeled as I^+ and I^-). The distance ℓ_c between current leads is 15.43 μm, the separation ℓ_v between the voltage leads 1 and 2 is 9.37 μm, while the average width w of the flake is 6.77 μm. (b) Sketch of one of our devices when measured in a two-terminal configuration, although the sample resistivity $\rho_{xx} = V_{12}/I_{ds}$ was measured by using a 4-terminal configuration where V_{12} is the voltage between contacts 1 and 2 resulting from the current I_{ds} injected through the drain (D) and source (S) current contacts. The Hall response was measured through contacts 1 and 3 with the magnetic field applied perpendicularly to the plane of the sample/substrate. (c) Atomic force microscopy image (top view) across the edge of the device previously shown in (a). Blue line indicates the line along which the height profile shown in (d) was measured. (d) Height profile across the edge of the device indicating a thickness of ≃70 Å or approximately 10 atomic layers. (e) Atomic resolution transmission electron microscopy image ([110] plane) of a multilayered $MoSe_2$ crystal from the same batch used for the electrical transport measurements discussed here, displaying both the Se and Mo atoms. (f) Electron diffraction pattern of a single atomic layer indicating a high degree of crystallinity.

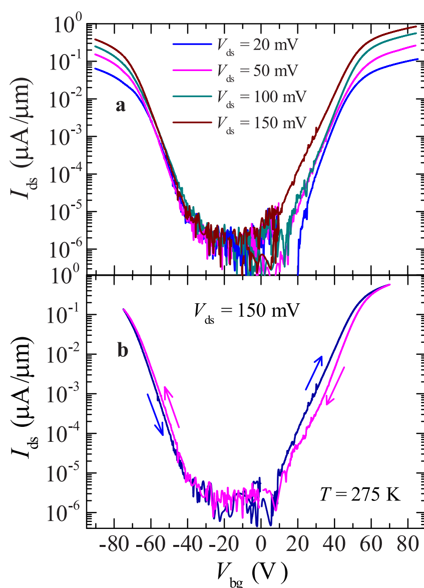

Figure 2. (a) Electrical current I_{ds} flowing through the drain-source contacts normalized by the width of the channel as a function of the back-gate voltage V_{bg} for several (constant) values of the excitation voltage V_{ds} across the current leads. (b) I_{ds} as a function of both increasing (blue line) and decreasing (magenta line) values of V_{bg}. Notice that for both electrons ($V_{bg} > 0$) and holes ($V_{bg} < 0$) the ratio between the transistor current "on" to "off" state is $\sim 10^6$. A small hysteresis is observed, suggesting the formation of domains containing either electrons or holes and whose size is gate-voltage dependent.

reason all results shown in this manuscript were collected under a maximum excitation voltage V_{ds} = 150 mV.

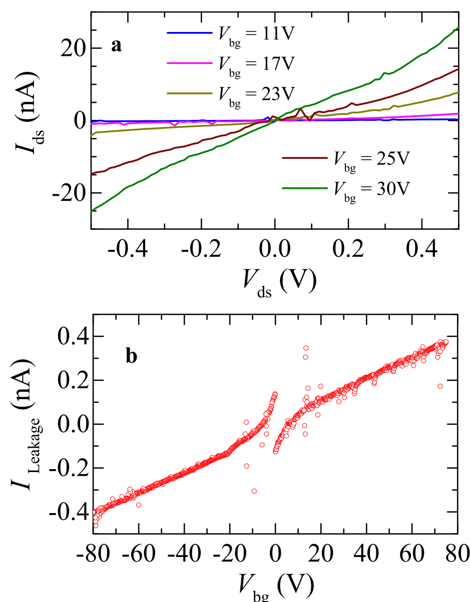

Figure 3. (a) I_{ds} as a function of the excitation voltage V_{ds} for several constant values of the gate voltage V_{bg}. Notice how $I_{ds}(V_{ds})$ is nearly linear for V_{ds} < 200 mV. (b) Typical leakage current $I_{leakage}$ through the back-gate as a function of V_{bg}. Notice that $I_{leakage}$ always remains below 1 nA even when I_{ds} surpasses 1 μA (see Figure 2).

Figure 3b, shows a typical trace of the current $I_{leakage}$ leaking through the back gate as V_{bg} is swept from −80 up to 75 V. As seen, although the current through the channel can surpass 1 μA, $I_{leakage}$ never surpasses 0.5 nA.

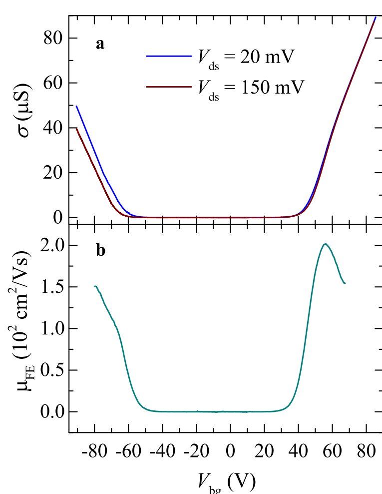

Figure 4. (a) Conductivity $\sigma = I_{ds}w/V_{ds}\ell$ as a function of the back-gate voltage V_{bg} for two constant values of the excitation voltage V_{ds}, or respectively 20 and 150 mV applied across the current leads. Notice that both curves collapse into a single curve for positive gate voltages, thus indicating linear regime, but not for $V_{bg} < 50$ V. (b) Field-effect mobility $\mu_{FE} = c_g^{-1}\ d\sigma/dV_{bg}$, where c_g^{-1} is the gate capacitance, as a function V_{bg}.

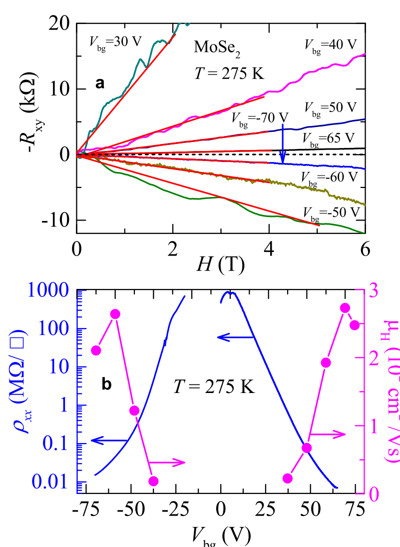

Figure 5. (a) Raw Hall resistance $R_{xy} = V_{13}/I_{ds}$, where V_{13} is the voltage across contacts 1 and 3 in Figure 1a, as a function of the magnetic field H and for several values of the back-gate voltage V_{bg}. Red lines are linear fits from whose slope we extract the Hall constant $R_H = 1/ne$ where n is the number of carriers. (b) Resistivity $\rho_{xx} = V_{12}w/I_{ds}\ell$, where V_{12} is the voltage across contacts 1 and 2 in Figure 1a, and Hall mobility $\mu_H = R_H/\rho_{xx}$ as a function of V_{bg}. Notice how μ_H approaches ~250 cm^2/(V s) for both electrons and holes.

Figure 4a displays the two-terminal conductivity $\sigma = I_{ds}\ell_c/V_{ds}w$ as a function of V_{bg} for two values of the excitation voltage V_{ds}, *i.e.*, respectively 20 and 150 mV. As seen, for $V_{bg} > 0$ V both curves collapse on a single curve indicating linear regime, although this is not the case for negative values of V_{bg}. It is important to emphasize that this linear regime does not indicate ohmic contacts: it indicates that thermally excited carriers can flow above the Schottky barriers due to thermionic emission, thus behaving as if the contacts were ohmic.[20] Another important observation in the plot of I_{ds} as a function of V_{bg} in a linear scale, is the existence of threshold gate voltages, *i.e.*, $V_{bg}^t \sim +35$ and -50 V for the conduction of electrons and holes, respectively. In several recent manuscripts it was discussed that disorder, either inherent to the material as for example chalcogenide vacancies (up to 10^{13} cm^{-2}),[21] or resulting from surface roughness and charge traps at the interface, leads to carrier localization and therefore to two-dimensional variable range hopping conductivity (2DVRH) in MoS_2.[21,22] Notice that similar behavior is observed at the interface between Si and SiO_2 and is discussed at length by Ando *et al.*[23] We observed also 2DVRH when studying the temperature dependence of the conductivity in either WSe_2 or $MoTe_2$ exfoliated onto SiO_2, concluding that the V_{bg}^t results from an interplay between disorder-induced carrier-localization, thermally activated detrapping processes, and the screening of charge-traps by gate accumulated carriers.[24,25] Lower temperatures are unfavorable for thermally activated detrapping leading to an increase in V_{bg}^t, as observed experimentally. To decrease V_{bg}^t one would need a smoother interface/substrate, to improve the fabrication processes in order to reduce the amount of spurious charges at the interface, and to reduce the number of point defects present in the material.

Figure 4b shows the resulting two-terminal field-effect mobility, *i.e.*, $\mu_{FE} = 1/c_g\,|d\sigma/dV_{bg}|$ as a function of V_{bg}, where $c_g = 12.783 \times 10^{-9}$ F/cm^2 is the capacitance between the gate and the channel for a 270 nm thick SiO_2 layer ($c_g = \varepsilon_0\varepsilon_r/d$ where $\varepsilon_r = 3.9$ and $d = 270$ nm). The extracted two-terminal field-effect mobility is observed to reach maximum values of ~200 cm^2/(V s) for electrons and ~150 cm^2/(V s) for holes, which compares well with values ranging from 100 to 150 cm^2/(V s) previously extracted by us for multilayered MoS_2 on SiO_2.[26] We measured two-terminal field-effect mobilities in 10 devices, all showing ambipolar behavior and field-effect mobilities ranging between 100 and 150 cm^2/(V s). But as we discussed in ref 26, two-terminal measurements tend to be dominated by the quality and the resistance of the contacts due to the Schottky barriers and often yields lower mobilities than the values that one would extract from 4 terminal measurements. To circumvent this issue we evaluated the mobilities of this FET through the Hall effect measurements shown below.

Figure 5a shows the raw Hall resistance $R_{xy}(H) = (V_H(+H) - V_H(-H))/2I_{ds}$ as a function of the magnetic-field H, where the Hall voltage $V_H(H) = V_{13}(H)$ corresponds to the voltage measured between voltage contacts 1 and 3 as the field is swept from 0 to a finite value. Notice (i) how R_{xy} changes its sign when one changes the sign of V_{bg} and (ii) that one cannot extract any Hall response for V_{bg} values between ±40 V indicating

the near total absence of mobile carriers within the channel. The fact that the transistor can be fully depleted indicates that only one type of carrier is present at any given gate voltage. Red lines are linear fits from which we extracted the Hall constant $R_H = R_{xy}/H = 1/ne$, where $n = n_h$ or n_e is the number of either holes or electrons as extracted from negative and positive gate voltages, respectively. We emphasize that the clear correlation between the sign of the Hall response and the sign of V_{bg} is consistent with the presence of only one type of carrier within the conducting channel. This should not be surprising, since one expects the gate electric field to easily displace the position of the Fermi level toward either the conduction or the valence band (whose indirect band gap was recently measured[27] to be 1.41 eV). The simultaneous presence of both types of carriers with distinct mobilities would not be easily reconciled with the linear dependence of R_H on H. Figure 5b shows both the four-terminal resistivity ρ_{xx} (blue line) and the resulting Hall mobility μ_H (magenta markers) for both carriers as a function of the gate voltage. As seen, the Hall mobility is nearly zero for -37 V < V_{bg} < $+37$ V reaching maximum values of $\sim$250 cm^2/(V s) for $V_{bg} = -60$ V and $\sim$260 cm^2/(V s) for $V_{bg} = +60$ V, respectively. These values are comparable to the room temperature 4-terminal field-effect electron mobility measured by us[26] in MoS_2. However, among several samples the mobilities can vary by a factor as large as three; see the Supporting Information for Hall mobility results from another, more typical, multilayered $MoSe_2$ sample, showing lower Hall mobility values.

Our previous Hall effect studies[24,25] on hole-doped WSe_2 and on hole-doped $MoTe_2$ revealed a carrier density n which as expected, is linearly dependent on the gate voltage: $n = c_g V_{bg}/e$. In both cases, a linear fit of $n(V_{bg})$ to extract the effective gate capacitance c_g^* yields higher values than the ones expected from the dielectric constant of SiO_2, indicating the existence of spurious charges in the conduction channel. However, as seen in Figure 6, which displays n as extracted from the Hall effect as a function of V_{bg}, n is not perfectly linear on V_{bg}, particularly for gate voltages close to the threshold value. This deviation from linearity can probably be ascribed to the aforementioned interplay between disorder-induced charge-localization, thermally activated detrapping, and the screening of spurious charges in the channel by the accumulation of gate-induced carriers. Linear fits (red lines) to both the hole and the electron branches yields $c_g^* = (9.2 \pm 3.3) \times 10^{-9}$ and $(23 \pm 6) \times 10^{-9}$ F/cm^2 for holes and electrons, respectively. The larger value for c_g^*, as extracted from the electron branch, relative to the ideal value c_g = 12.783 $\times 10^{-9}$ F/cm^2 indicates an excess of negative charges in the channel. These can be neutralized by the addition of holes, thus explaining the proximity in value between c_g and c_g^* as extracted from the hole branch. Improvement in carrier conduction through the contacts (perhaps by making the contacts *via* the stacking with another van der Waals solid such as graphene[28]), in charge screening (*e.g.*, with the use of a high κ dielectrics) or in reducing the spurious charges in the channel during the fabrication process, should further increase the carrier mobility and reduce the threshold gate voltage required for carrier conduction. Such improvements, coupled to a better control on the amount of point defects, could make $MoSe_2$ a very promising candidate for low-power and low-cost complementary electronics. Notice that if one used the values for the gate capacitance as extracted from the Hall effect measurements, one would obtain smaller values for the maximum field-effect electron mobilities.

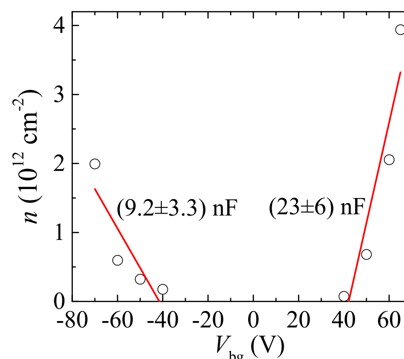

Figure 6. Density of carriers $n = eR_H$ for our $MoSe_2$-based FET as a function of V_{bg}. Red lines are linear fits from which we evaluate the effective gate capacitances $c_g^* = (9.2 \pm 3.3) \times 10^{-9}$ and $(23 \pm 6) \times 10^{-9}$ F/cm^2 for holes and electrons, respectively.

CONCLUSIONS

$MoSe_2$ grown by chemical vapor transport using iodine as the transport agent, when mechanically exfoliated onto SiO_2, and electrically contacted by using a combination of Ti and Au, behaves as an ambipolar semiconductor in contrast to electron-doped[1] MoS_2 and hole-doped[25] $MoTe_2$. Therefore, for samples mechanically exfoliated onto SiO_2 and electrically contacted with Ti:Au, the electrical response evolves from electron doped (MoS_2), to ambipolar ($MoSe_2$) to hole doped ($MoTe_2$) as the size of the semiconducting gap decreases.[29] Although this evolution (or tunability) has yet to be understood, this trend could have interesting implications since heterogeneous, van der Waals coupled stacks have the potential to lead to a wide variety of semiconducting heterojunctions and superlattices. For example, the unique optical properties of transition metal dichalcogenides make them promising candidates for photodetectors, photodiodes, photovoltaics and even light-emission.[5,6,30−35] The distinct band gaps coupled to the tunability of the work functions of the metallic contacts, also open the possibility of engineering the band gaps of their heterostructures.[36] Furthermore, as recently shown,[37] the stack of distinct

atomically thin layers of transition metal dichalcogenides to create $p-n$ junctions (which are fundamental components in modern electronics[38]), possessing nearly perfect interfaces, can lead to unique platforms for novel, high-performance electronic and optoelectronic devices. In effect, a photovoltaic solar cell, photodiode like response, and a light emitting diode were recently demonstrated[39−41] from $p-n$ junctions fabricated from just a single-layer of *ambipolar* WSe_2. Therefore, our results indicate that $MoSe_2$ is another excellent candidate, for not only complementary logic electronics, but also for $p-n$ junctions based on a single atomic layer. So far, at room temperature and on SiO_2, our preliminary studies reveal very similar carrier mobilities between both ambipolar $MoSe_2$ and hole-doped WSe_2.[24] This is somewhat surprising given the very sizable difference in atomic masses between Mo and W, which affects the frequency of the phonon modes and consequently, of the concomitant strength of the electron−phonon coupling, claimed to be the main limiting factor for the room temperature carrier mobility in these systems. We conclude that the mobilities shown here are limited not only by phonons, but also by extrinsic factors such as the interaction with substrates, quality of the contacts, spurious charges in the channel, *etc*. Therefore, our room temperature mobility values are improvable, which would lead to an increase in the performance of the aforementioned electronic and optoelectronic devices based on transition metal dichalcogenides.

METHODS

$MoSe_2$ single-crystals were synthesized through a chemical vapor transport technique using iodine as the transport agent. Multilayered flakes of $MoSe_2$ were exfoliated from these single-crystals by using the micromechanical exfoliation technique and transferred onto *p*-doped Si wafers covered with a 270 nm thick layer of SiO_2. For making the electrical contacts 90 nm of Au was deposited onto a 4 nm layer of Ti *via* e-beam evaporation. Contacts were patterned using standard e-beam lithography techniques. After gold deposition, these devices were annealed at 250 °C for ∼2 h in forming gas. This was followed by a subsequent high vacuum annealing for 24 h at 120 °C. Atomic force microscopy (AFM) imaging was performed using the Asylum Research MFP-3D AFM. Electrical characterization was performed by using a combination of sourcemeter (Keithley 2612 A), Lock-In amplifier (Signal Recovery 7265) and resistance bridges (Lakeshore 370) coupled to a conventional ^{4}He cryostat and a 15 T magnet. The sample was kept under a low pressure of ^{4}He as exchange gas. Energy dispersive spectroscopy, to verify the stoichiometry, was performed through field-emission scanning electron microscopy (Zeiss 1540 XB). Sub-Angstrom aberration corrected transmission electron microscopy was performed by using a JEM-ARM200cF microscope. EDS was performed through field-emission scanning electron microscopy (Zeiss 1540 XB).

Conflict of Interest: The authors declare no competing financial interest.

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Supporting Information Available: I_{ds} as a function of V_{bg} characteristics, Hall effect, density of carriers and Hall mobilities for a second few-layered $MoSe_2$ crystal. Also typical EDS spectra of a chemical vapor transport grown $MoSe_2$ single crystal. This material is available free of charge *via* the Internet at http://pubs.acs.org.

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